



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/089,535	08/05/2002	Wenshun Tian	851663.434USPC	5003
500	7590	03/31/2006	EXAMINER	
SEED INTELLECTUAL PROPERTY LAW GROUP PLLC 701 FIFTH AVE SUITE 6300 SEATTLE, WA 98104-7092			HAN, QI	
			ART UNIT	PAPER NUMBER
			2626	

DATE MAILED: 03/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/089,535

Applicant(s)

TIAN ET AL.

Examiner

Qi Han

Art Unit

2654

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/27/2002.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

U.S.C. National Stage Application

1. Acknowledgement is made of the indication that the present application is filed under 35 U.S.C. 371, of the indication that the required form PCT/DO/ED/903 is present, and of the use of transmittal form PCT/DO/EO/1390. Thus, the present application is being treated as a filing under 35 U.S.C. 371.

Information Disclosure Statement

2. The references listed in the Information Disclosure Statement submitted on 11/27/2002 have been considered by the examiner (see attached PTO-1449).

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2654

4. Claims 1-2, 5-9 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over SATO et al. (6,201,488 B1) hereinafter referenced as SATO.

As per **claim 1**, SATO discloses CODEC for consecutively performing a plurality of algorithms (title), comprising:

“a digital signal processor (DSP)”, (Figs. 4-5, ‘DSP’ and ‘DSP core’; col. 2, lines 6-7, ‘a CODEC having a DSP’);

“a first memory coupled to the DSP and containing an instruction code program, the function of each codes being performed by the DSP, in use, according to said instruction code program”, (col. 2, lines 9-17, ‘a codec comprising a data processing unit performing an encoding/decoding operation (function of codecs) on a digital signal’, ‘a program memory storing (containing) a program divided into a plurality of block programs (instruction code program’);

“a second memory coupled to the DSP and partitioned to include a plurality of separate memory segments” (col. 2, lines 18-21, ‘a data memory storing a set of data...being divided (partitioned) into a plurality of data blocks (segments)’);

“codec” “implemented using the DSP by running said instruction code program in said first memory [a plurality of times in re-entrant instances], and wherein each codes instance is provided access to a respective separate memory segment in said second memory for storing data used in encoding/decoding a respective separate data stream”, (col. 2, lines 22-39, ‘executing (implementing or running) each block program stored in the program memory by using a corresponding data block stored in the data memory’, ‘a plurality of programs (algorithms) can be consecutively performed when the CODEC is operated over a plurality of phases’).

But, SATO does not expressly teach using multiple “codecs” running “a plurality of times in re-entrant instances”. However, this feature is well known in the art as evidenced by SATO himself who further discloses that ‘DSP...can execute the same program by referring to different work data (corresponding to a plurality of times in re-entrant instances)’ (col. 7, lines 44-45), and providing ‘work data ...sequentially rewritten (re-entrant instance) on an individual bank basis’ and ‘multi-algorithm process’ and processing multiple ‘channels (corresponding to a plurality of codecs)...and the work data used when the programs corresponding to each channel is executed’ (col. 10, lines 19-42; also see Figs 8, 13 and 18), wherein processing signal for each channel corresponding to the claimed “the function of each codec being performed”, which suggests that SATO’s system has capability to implement the codec function for multiple channels (multiple codecs) with rewriting work data multiple times in sequential manner as claimed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify SATO by specifically providing implementation of codec function for multiple channels (multiple codecs) with rewriting work data multiple times in sequential manner, as taught by Wang, for the purpose of performing a multi-channel process for the system (SATO: col. 10, lines 47-48).

As per **claim 9** (depending on claim 8), SATO further discloses “a third memory coupled to said DSP which is accessible by each of the codes instances for shared storage of temporary variables and data buffering in encoding/decoding said respective separate data streams” (Figs. 16 and 18 and col. 11, lines 39-57, ‘work area work#0 (third memory) is a temporary work area’ ‘accessing (buffering) the same area of the data memory in each phase (including separate data

Art Unit: 2654

streams)', which suggests that SATO's system has capability of implementing the claimed feature).

As per **claim 12** (depending on claim 8), SATO further discloses "each of the memory segments in said second memory is the same size" (Figs. 10-11 and 14, col. 8, lines 34-47, 'memory area of the RAM includes the five banks (implying each bank as the same size) ... each of which stores a single data block').

As per **claim 13** (depending on claim 8), SATO further discloses "wherein said first memory is provided with a plurality of instruction code programs for implementing different kinds of codecs, and wherein different codes instances may be selected from the different kinds of codes" (col. 2, lines 6-8, 'a DSP which can consecutively execute a plurality of algorithms (interpreted as implementing different kinds of codecs)'; col. 2, line 62 to col. 3, lines 4, 'the program changing unit may store the new data... the block program ...is replaced with a new program block....a plurality of algorithms can be performed ...in of the banks sequentially selected').

As per **claim 14** (depending on claim 13), SATO further discloses "wherein each of the memory segments in said second memory is the same size, and the size of the memory segments is selected according to the maximum memory required by any of the plurality of different kinds of codes", (Figs. 10-11 and 14, col. 8, lines 34-47, 'memory area of the RAM includes the five banks (implying each bank as the same size) ... each of which stores a single data block'); col. 17, lines 37-40, 'the work data...is not fixed' and 'the start address and the end address of the memory area of the work data are determined for each phase', which suggests SATO's system has capability of implementing the claimed feature).

Regarding claims 1-2 and 5-7, they recite a method. The rejection is based on the same reason described for claims 8-9 and 12-14 respectively, because the claims recite the same or similar limitation(s) as claims 8-9 and 12-14 respectively.

5. Claims 3-4, 10-11 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over SATO as applied to claims 1 and 8, and further in view of KLAAS et al. (6,628,999 B1) hereinafter referenced as KLAAS.

As per **claim 10** (depending on claim 8), SATO further discloses “each codec instance accesses the corresponding memory segment [using indirect addressing] based on at least one index register, the at least one index register being set for each codec instance to modify addressing of variables for that codes instance to the corresponding memory segment” (Figs. 10-11, 18 and 26 and col. 12, lines 25-52, ‘DSP core can always access one of the sets of work data...by providing an offset address to an offset resister (corresponding to index register)’, ‘calculates base address’ using ‘variable K’).

But, SATO does not expressly disclose whether or not using “indirect addressing”. However, this feature is well known in the art as evidenced by KLAAS who discloses single-chip audio system volume control circuitry and methods (title), comprising ‘the address of the indirect register accessed by the indexed data register’ (col. 81, lines 4-6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify SATO by specifically providing the address of the indirect register accessed by the indexed data register, as taught by KLAAS, for the purpose of offering more available mode of addressing for the system (KLAAS: col. 81, lines 4-8).

Art Unit: 2654

As per **claim 11** (depending on claim 10), SATO in view of KLAAS further discloses "the plurality of memory segments are contiguous in said second memory, and said at least one index register is set for each codec instance according to an offset based on the difference in address from a first of said memory segments to the memory segment corresponding to that codes instance" (SATO: Figs. 5 and 16, col. 12, lines 25-52, 'DSP core can always access one of the sets of work data...by providing an offset address to an offset register (corresponding to index register)', 'calculates base address $XBAS + XBNK \times K$ ' using 'variable K').

Regarding **claims 3-4** (depending on claim 1), the rejection is based on the same reason described for claims 10-11 respectively, because the claims recite the same or similar limitation(s) as claims 10-11 respectively.

Regarding **claim 16**, the rejection is based on the same reason described for claims 8 and 10, because the claim recites the same or similar limitations as claims 8 and 10.

Regarding **claim 15**, it recites a method. The rejection is based on the same reason described for claim 16, because the claim recites the same or similar limitations as claim 15.

Conclusion

6. Please address mail to be delivered by the United States Postal Service (USPS) as follows:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to: 571-273-8300, (for formal communications intended for entry)

Or: 571-273-8300, (for informal or draft communications, and please label "PROPOSED" or "DRAFT")

If no Mail Stop is indicated below, the line beginning Mail Stop should be omitted from the address.

Art Unit: 2654

Effective January 14, 2005, except correspondence for Maintenance Fee payments, Deposit Account Replenishments (see 1.25(c)(4)), and Licensing and Review (see 37 CFR 5.1(c) and 5.2(c)), please address correspondence to be delivered by other delivery services (Federal Express (Fed Ex), UPS, DHL, Laser, Action, Purolater, etc.) as follows:

U.S. Patent and Trademark Office
Customer Window, Mail Stop _____
Randolph Building
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qi Han whose telephone numbers is (571) 272-7604. The examiner can normally be reached on Monday through Thursday from 9:00 a.m. to 7:00 p.m. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richemond Dorvil, can be reached on (571) 272-7602.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Inquiries regarding the status of submissions relating to an application or questions on the Private PAIR system should be directed to the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028 between the hours of 6 a.m. and midnight Monday through Friday EST, or by e-mail at: ebc@uspto.gov. For general information about the PAIR system, see <http://pair-direct.uspto.gov>.

QH/qh
March 9, 2006


RICHEMOND DORVIL
SUPERVISORY PATENT EXAMINER